OIPE JC184
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PATENT & TRADEMARK OFFICE

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Kinsman et al.

Serial No.: 09/917,127

Filed: July 27, 2001

For: METHOD FOR FABRICATING A CHIP SCALE PACKAGE USING WAFER LEVEL PROCESSING AND DEVICES RESULTING THEREFROM

Confirmation No.: 3326

Examiner: M. Trinh

Group Art Unit: 2822

Attorney Docket No.: 2269-3572.1US
(97-1243.01/US)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

July 7, 2003
Date

Signature

Leah J. Barrow
Name (Type/Print)

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO/SB/08 be considered by the Examiner and made of record. Copies of the listed documents are enclosed pursuant to 37 C.F.R. § 1.98(a). The listed documents were cited by the Office in co-pending application Serial No. 09/586,243, filed on June 2, 2000, and directed to a related invention

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicants herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

U.S. Patent Documents

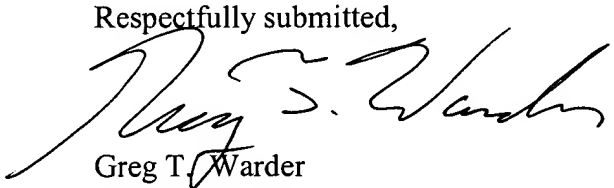
U.S. Patent No.	Publication Date	Patentee
US - 5,867,417	02/02/1999	Wallace et al.
US - 5,844, 779	12/01/1998	Choi

Applicants offer to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is filed after the mailing date of the first Office Action on the merits.

I hereby certify that no item of information contained in the Supplemental Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of the statement, and therefore no fee is due.

Respectfully submitted,



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Date: July 7, 2003
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THE PATENT & TRADEMARK OFFICE MAILROOM DATE STAMPED HEREON IS AN ACKNOWLEDGEMENT THAT ON THIS DATE THE PATENT & TRADEMARK OFFICE RECEIVED:

Supplemental Information Disclosure Statement (2 pages); and Form PTO/SB/08 (1 page), with copy of cited reference (1 document)

Invention:	METHOD FOR FABRICATING A CHIP SCALE PACKAGE USING WAFER LEVEL PROCESSING AND DEVICES RESULTING THEREFROM
Applicant(s):	Kinsman et al.
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Serial No.:	09/917,127
Date Sent:	April 7, 2003 via first class mail
Docket No.:	2269-3572.1US
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